A 22 TO 24 GHZ CRYOGENICALLY COOLED LOW NOISE FET AMPLIFIER IN COPLANAR WAVEGUIDE

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SUMMARY

This paper describes the design and development of a 22 to 24 GHz Cryogenically Cooled Amplifier with a noise temperature of 150K and a gain of 33 dB at 23 GHz when the amplifier is cooled to 77K.

INTRODUCTION

In recent years, GaAs FET amplifiers have found widespread application in low noise microwave receiving systems. Noise temperatures comparable to those achieved with paramps have been reported with cryogenically cooled FET amplifiers.

The amplifier to be described relies on a comprehensive transistor model that was derived from S-parameter measurements made below the band of operation. This model was used to design a cascadable single-stage amplifier with a gain of 4 dB minimum and a noise figure less than 4.6 dB at 290K.

To the authors' knowledge, this is the first report of a cryogenically cooled FET amplifier in the 22 to 24 GHz range.

TRANSMISSION MEDIUM

Coplanar waveguide was chosen over microstrip as a transmission medium for the following reasons:[1,2]

- It allows the circuit designer to realize both low and high impedance lines without the need for excessively wide or narrow conductor strips.
- Parasitic source grounding inductance is minimized since the ground plane is very close to the FET. This feature coupled with the single-mode transmission property of coplanar waveguide allows one to achieve high reverse isolation (S12) at K-band frequencies.
- Another advantage of this transmission medium is its ability to handle both series and shunt circuit elements easily.

A cross section of coplanar waveguide is shown in Figure 1. The characteristic impedance (Z_o) is inversely proportional to the aspect ratio S/(S + 2W).

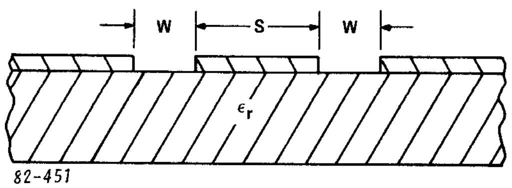

Figure 1. Coplanar Waveguide

TRANSISTOR MEASUREMENTS AND CHARACTERIZATION

Since K-band S-parameter data was not available for the Mitsubishi MGFC-1403 transistor, S-parameter measurements were a critical first step in the design. Direct measurement of S-parameters at K-band frequencies could not be done because of equipment limitations. Therefore, extrapolation of data measured at lower frequencies was considered.

In order to reliably extrapolate such data, a comprehensive model was created for the transistor. This was done by mounting the FET in a coplanar 50 Ω system and measuring the S-parameters of the device using standard automatic measurement techniques. Reliable data was obtained from 2 to 15 GHz.

This information was then entered in a computer file containing the circuit model shown in Figure 2. The program varied several key elements in the file striving to make the circuit analysis match the measured S-parameters. After optimization, the model tracked the measured S-parameter data quite closely. The model was then analyzed up to 30 GHz, yielding reliable S-parameter data for circuit design. To verify the validity of the device model, slotted line measurements of S_{11} and S_{22} were performed at 22 to 24 GHz. These measurements agreed quite closely with the predicted S_{11} and S_{22}.

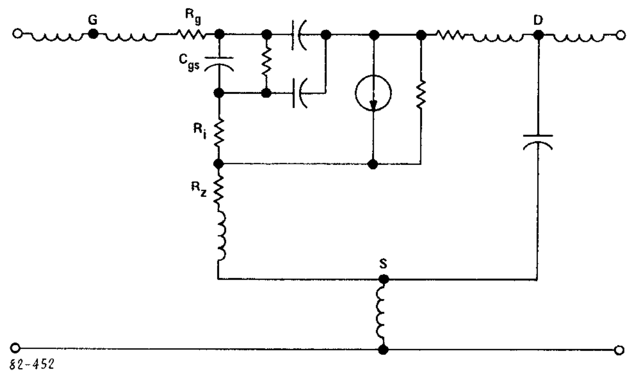

Figure 2. Transistor Model

NOISE MODEL

After the device model was obtained, the model was analyzed to predict the optimum source admittance for minimum noise figure. This was done by creating a simplified noise model from the device model already obtained.[3] The model is shown in Figure 3, and the corresponding equations (1) through (4) are as follows:

$$g_1 = \frac{1}{(Q_1^2 + 1)\, R_1} \quad (1)$$

and

$$C_1 = \frac{Q_1^2\, C_{gs}}{(Q_1^2 + 1)} \quad (2)$$

$$R_1 = R_g + R_i + R_z \quad (3)$$

and

$$Q_1 = \frac{1}{2\pi\, fc\, R_1\, C_{gs}} \quad (4)$$

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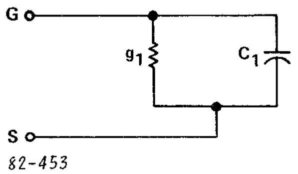


Figure 3. Noise Model

The values R_g, R_i, R_z, and C_{gs}, needed to calculate R_1 and Q_1, are element values obtained from the transistor model shown in Figure 2. Once values g_1 and C_1 were obtained, the optimum source admittance, ($Y_{sopt} = g_{sopt} + jb_{sopt}$) was calculated using equations (5) and (6).

$$g_{sopt} = g_1 \sqrt{1 + \frac{1}{A}} \tag{5}$$

$$b_{sopt} = -\omega C_1' = \left(\frac{-Q_1}{Q_1^2 + 1} \right) \omega C_1 \tag{6}$$

The quantity A is derived from the minimum attainable noise figure (F_{min}) of the device at the frequency of interest through equation (7).

$$A = \frac{(F_{min} - 1)^2}{4 F_{min}} \tag{7}$$

The derivations for equations (1) through (7) can be found along with a complete description of the noise modeling technique in reference 3. The F_{min} at 23 GHz was estimated to be 3.75 dB by extrapolating the manufacturer's data. It was found that, at K-band frequencies, the source admittance required for minimum noise figure is very close to the admittance required for maximum power transfer. Therefore, at K-band the maximum available gain (G_{max}) approaches the associated gain (G_{NF}) for the transistor.

CIRCUIT DESIGN

A computer analysis of the circuit in Figure 2 yielded the device S-parameters shown in Table 1. Included in the table is the optimum generator reflection coefficient for minimum noise figure at 23 GHz. This was found from the noise model already described. Smith Chart techniques were used to design input and output matching networks. Computer optimization was then used to obtain minimum noise figure and flat gain. During a subsequent out-of-band analysis, it was found that a gain peak existed at around 6 GHz. A decoupling network was incorporated in the gate and drain bias circuits to reduce the gain peak. In order to achieve additional rejection at 6 GHz, a band-pass filter module was designed. The filter is cascaded with the amplifier modules in the complete assembly. The final, optimized circuit is shown in Figure 4 and results of the circuit analysis appear in Table 2. The noise figure analysis at 23 GHz is included in this table.

CONSTRUCTION

The amplifier circuit was built with distributed and lumped elements. The capacitors selected were low loss parallel plate types. Required inductances were achieved with bond wires or ribbons. Transmission lines and resistors were photoetched on a 0.015-inch Au-Cr-deposited alumina substrate. The chrome adhesion layer provided adequate sheet resistance for the thin film resistors.

Table 1. Transistor Parameters

Frequency (GHz)	S_{11}	S_{21}	S_{12}	S_{22}	Γ_{opt}
22	0.63/157°	1.15/28.5°	0.137/24°	0.35/-130°	
23	0.64/152°	1.10/24.7°	0.141/25°	0.36/-137°	0.63/+144°
24	0.65/148°	1.06/21.0°	0.145/26°	0.36/-144°	

Table 2. Amplifier Circuit Analysis

Frequency (GHz)	S_{11}	S_{21}	S_{12}	S_{22}	S_{21} (dB)	Noise Figure (dB)
22	0.33/86°	1.60/-133°	0.19/-137°	0.19/91°	4.06	--
23	0.23/20°	1.61/-159°	0.21/-160°	0.07/29°	4.13	3.96
24	0.32/-45°	1.51/175°	0.21/180°	014/-85°	3.55	--

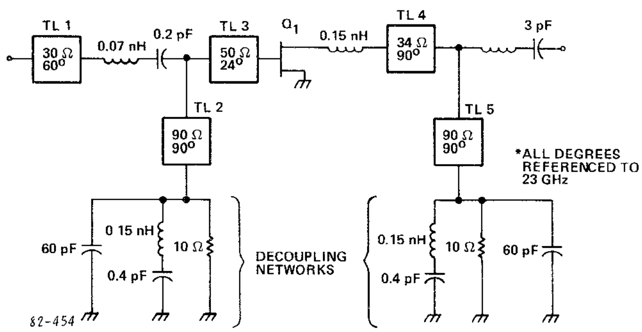


Figure 4. Amplifier Circuit

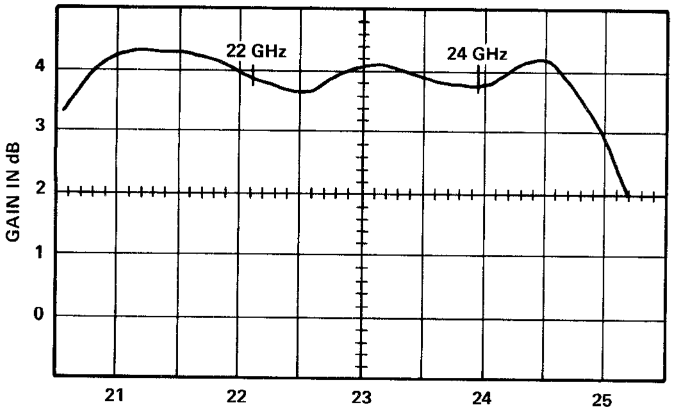
Kovar was chosen as the carrier and amplifier housing material because of its excellent thermal stability and close compatibility with alumina over the wide temperature range. Kovar also lends itself to electron beam welding which is used to hermetically seal the amplifier.

MODULE MEASUREMENTS

Gain and return loss were measured using standard swept measurement techniques. Noise figure was measured using an extremely low noise parametric amplifier as a second stage to minimize measurement uncertainty. The AIL-developed parametric amplifier provided a noise figure of 2.6 dB and 28 dB of gain at 23 GHz, at 300K ambient.

DISCUSSION OF MODULE RESULTS

Figure 5 shows the measured gain versus frequency of the amplifier module mounted in a test fixture. The test fixture connectors each have about 0.25 dB loss at K-band. Therefore, the minimum gain of the circuit is approximately 4.1 dB at 24 GHz. The measured input VSWR of the single-stage amplifier is under 3.0:1 and the measured output VSWR is less than 1.7:1. The reverse isolation measured was greater than 17 dB from 22 to 24 GHz. The corrected noise figure of the FET amplifier module is shown in Table 3.



82-455

Figure 5. Measured Amplifier Module Gain

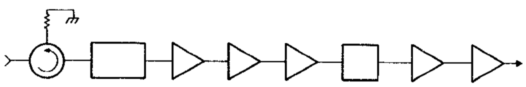
Table 3. Measured Single Stage Noise Figure

Frequency (GHz)	Noise Figure* (dB) at 25°C
22	4.6
23	4.6
24	4.5

*Includes second stage correction and correction for test fixture connector loss.

COMPLETE AMPLIFIER DESCRIPTION AND PREDICTED PERFORMANCE

The complete amplifier consists of five FET modules cascaded with one band-pass filter module and a through-line module as shown in the block diagram in Figure 6. Figure 7 is a photograph of the complete amplifier assembly. The through-line will be replaced with an additional FET module on units intended for room temperature use only. External isolators are placed at the input and output ports of the amplifier as shown in the block diagram (Figure 6).



	ISOLATOR	CONNECTOR	STAGE 1	STAGE 2	STAGE 3	BPF AND THROUGH-LINE	STAGE 4	STAGE 5	TOTAL
ROOM TEMP GAIN	-0.5 dB	-0.25 dB	+4.0 dB	+4.0 dB	+4.0 dB	-0.5 dB	+4.0 dB	+4.0 dB	18.75 dB
NET GAIN (ROOM TEMP)	0.89	0.94	2.5	2.5	2.5	0.89	2.5	2.5	72.7 = 18.6 dB
NOISE (K) (ROOM TEMP)	35.8	18.5	546.0	546.0	546.0	35.8	546.0	546.0	
NOISE CONTRIBUTION (ROOM TEMP)	35.8	20.8	652.6	261.0	104.4	2.7	46.9	18.8	1143°
*NET GAIN (77 K)	0.89	0.94	3.54	3.54	3.54	0.89	3.54	3.54	413.9 = 26.2 dB
**NOISE (K) (77 K)	9.5	4.9	109.2	109.2	109.2	9.5	109.2	109.2	
NOISE CONTRIBUTION (77 K)	9.5	5.5	103.5	52.2	20.9	0.7	9.4	3.8	232.5°

*GAIN AT 77 K IS ESTIMATED FROM PAST EXPERIENCE TO BE APPROXIMATELY 1.5 dB HIGHER THEN THE ROOM TEMPERATURE GAIN

**NOISE TEMPERATURE IS ESTIMATED FROM PAST EXPERIENCE TO BE 20% OF THE ROOM TEMPERATURE NOISE TEMPERATURE

82-456

Figure 6. Cascaded Amplifier Assembly Predicted Performance

The predicted mid-band performance of the amplifier is shown in Figure 6. A single stage unit with a mid-band gain of 4 dB and noise figure of 4.6 dB at room temperature was assumed for this calculation. The through-line loss was neglected in this estimate. Including isolator loss, the predicted gain is 26.2 dB and the predicted noise temperature is 232K for the cryogenically cooled amplifier.

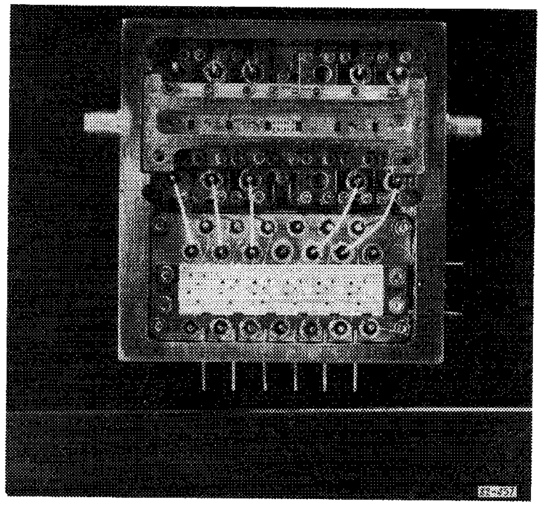


Figure 7. Complete Amplifier Assembly

CRYOGENIC AMPLIFIER MEASUREMENTS

Gain and noise temperature measurements were made using a CTI Refrigerator Model No. 1020R. The block diagram in Figure 8 describes the measurement setup. The area inside the dashed line represents the vacuum vessel which has waveguide input/output ports. Separate slotted line measurements were made on the sections labeled L1 through L6 to determine their individual losses. The diagram shows the physical temperature at which each section was maintained during the cryogenic measurements. The 189K temperature assigned to L2 and L5 is the estimated average temperature of the waveguide sections since they sustained a temperature gradient along their lengths. The reference for the gain measurement was taken outside the vessel (essentially at the input to L1), and the gain measurement was corrected for the losses listed in Figure 8. The noise temperature was measured using standard Hot/Cold Y-Factor measurement techniques and corrected for the losses described in Figure 8.

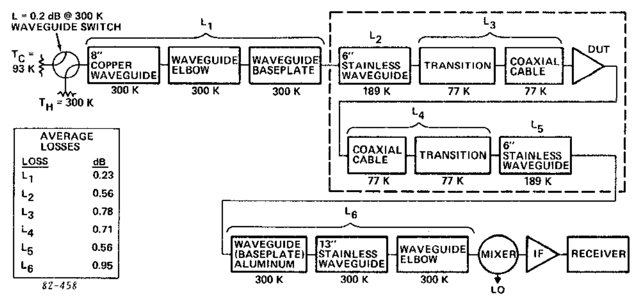


Figure 8. Cryogenic Measurement Setup

DISCUSSION OF AMPLIFIER RESULTS

The measured amplifier gain at 300K was 22 ±2 dB over the 22 to 24-GHz range. The measured noise temperature at 300K was 1134K maximum at 22 GHz, decreasing to 797K at 24 GHz.

The measured amplifier gain and noise temperature at 77K are shown in Figures 9 and 10. One difficulty was encountered when the amplifier was cooled. An out-of-band resonance below 22 GHz shifted up in frequency as the temperature was lowered. The resonance severely impacted the gain and noise temperature of the amplifier from 22.0 to 22.5 GHz. The cause(s) of this resonance has not been determined at the time of this writing. We observed degraded gain

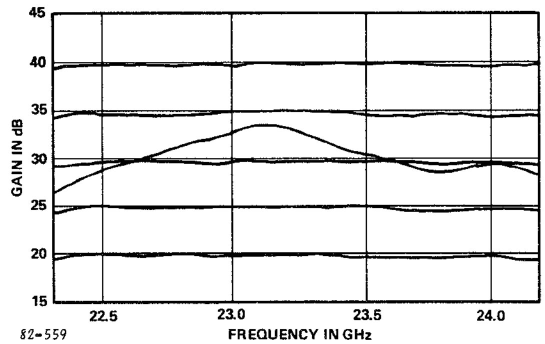


Figure 9. Amplifier Gain at T = 77K

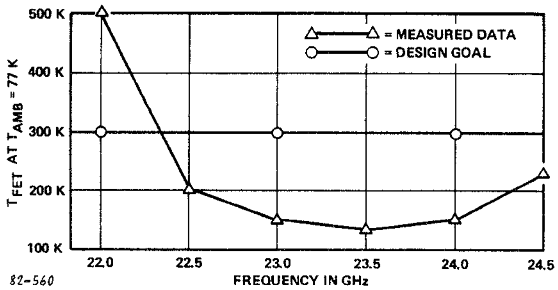


Figure 10. Measured Amplifier Noise Temperature at T = 77K

and noise temperature over this portion of the band. The noise temperature and gain were 504.6K and 22 dB, respectively, at 22 GHz. From 22.5 to 24.5 GHz, the measured noise temperature was determined to be 231.9K maximum, with a minimum of 136K occuring at 23.5 GHz. The noise temperature performance was well under the goal of 300K.

It is our belief that the observed resonance will present no fundamental obstacles in the achievement of the desired gain and noise temperature goals established for the amplifier. Improved results will be available in the near future.

CONCLUSION

Measured amplifier data shows that FET amplifiers can provide low noise performance at K-band fequencies. When cooled to cryogenic temperatures, the noise performance of FET amplifiers can approach that of room temperature parametric amplifiers.

The amplifier circuit described is readily adaptable to monolithic construction because of its small size (0.3 x 0.25 inch) and absence of interfacial grounds.

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